the number of transistors required for each gate, thus increasing the area and power consumption of each gate.

Accordingly, a need exists for a multiplexer for data shifting having reduced area and potentially other advantages.--

Replace the paragraphs beginning at page 3, line 7, with the following rewritten paragraphs:

--A logic circuit consistent with the present invention uses data sharing in a multiplexer for shifting data. It includes a plurality of logic gates and a plurality of shared data lines connecting the logic gates. Each logic gate receives data inputs and control signals, and the shared data lines provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates. In operation, the logic gates shift data received at the data inputs based upon the control signals and the connections of the shared data lines to produce a shifted data output.

A method consistent with the present invention includes sharing data among logic gates in a multiplexer for shifting data. It includes providing a plurality of logic gates each receiving data inputs and control signals, and connecting the logic gates using a plurality of shared data lines. The data lines provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates. Data received at the data inputs is shifted based upon the control signals and the connections of the shared data lines to produce a shifted data output.--

Replace the paragraph beginning at page 4, line 1, with the following rewritten paragraphs:

--FIG. 1 is a block diagram of a portion of a multiplexer illustrating data sharing consistent with the present invention; and--

Replace the paragraphs beginning at page 4, line 6, with the following rewritten paragraphs:

--A multiplexer consistent with the present invention uses data sharing among field-effect transistors (FETs) in order to reduce the number of transistors required by each logic gate. Therefore, instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines.

FIG. 1 is a block diagram of a portion 10 of a multiplexer for implementing data sharing consistent with the present invention. This example only illustrates four logic gates among many logic gates that may be required to implement a particular multiplexer depending upon the size of a data bus involved. This example illustrates four logic gates 11, 12, 13, and 14. Each logic gate receives data inputs, and produces shifted data outputs based